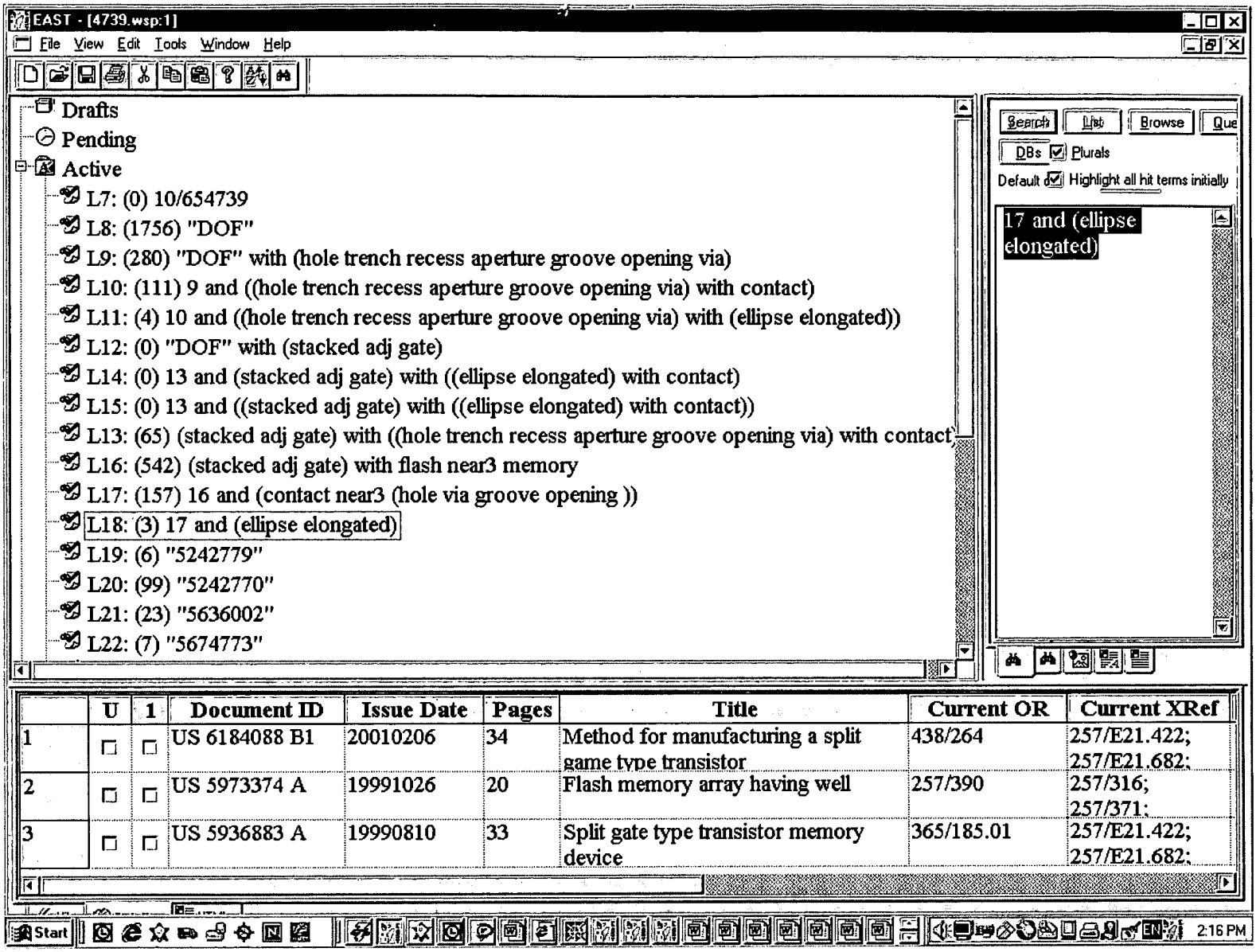


	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 6184088 B1	20010206	34	Method for manufacturing a split game type transistor	438/264	257/E21.422; 257/E21.682;
2	☐	☐	US 5973374 A	19991026	20	Flash memory array having well	257/390	257/316; 257/371;
3	☐	☐	US 5936883 A	19990810	33	Split gate type transistor memory device	365/185.01	257/E21.422; 257/E21.682;

EAST - [4739.wsp:1]

File View Edit Tools Window Help

L11: (4) 10 and ((hole trench recess aperture groove opening via) with (ellipse elongated))

L12: (0) "DOF" with (stacked adj gate)

L14: (0) 13 and (stacked adj gate) with ((ellipse elongated) with contact)

L15: (0) 13 and ((stacked adj gate) with ((ellipse elongated) with contact))

L13: (65) (stacked adj gate) with ((hole trench recess aperture groove opening via) with contact

L16: (542) (stacked adj gate) with flash near3 memory

L17: (157) 16 and (contact near3 (hole via groove opening))

L18: (3) 17 and (ellipse elongated)

Search | List | Browse | Que

DBs ☑ Plurals

Default ☑ Highlight all hit terms initially

(stacked adj gate) with ((hole trench recess aperture

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 20040057286 A1	20040325	40	Self-aligned split-gate NAND flash memory and fabrication process	365/185.17	
2	☑	☐	US 20030183883 A1	20031002	24	Non-volatile semiconductor memory device having memory cell array suita	257/390	257/E21.682; 257/E27.103;
3	☑	☐	US 20030113961 A1	20030619	21	Semiconductor device and manufacturing method thereof	438/157	257/E21.703; 257/E27.112
4	☑	☐	US 20030082879 A1	20030501	35	Non-volatile semiconductor memory device and method of manufacturing t	438/266	
5	☑	☐	US 20030008450 A1	20030109	13	Self-aligned process for a stacked gate RF MOSFET device	438/200	257/E21.627; 257/E23.019
6	☑	☐	US 20030003658 A1	20030102	12	Method of fabricating a non-volatile memory device to eliminate charge lo	438/257	
7	☑	☐	US 20020192906 A1	20021219	12	Method for forming a capacitor of a semiconductor device	438/255	257/E21.013; 438/398
8	☑	☐	US 20020171112 A1	20021121	24	Non-volatile semiconductor memory device having memory cell array suita	257/390	257/E21.682; 257/E27.103;
9	☑	☐	US 20020115310 A1	20020822	24	Etching mask, process for forming contact holes using same, and semico		257/499; 257/E21.577;
10	☑	☐	US 20020102793 A1	20020801	20	Method of fabricating a scalable stacked-gate flash memory device an	438/257	257/E21.689; 257/E27.081;

Start 2:17 PM

EAST - [4739.wsp:1]

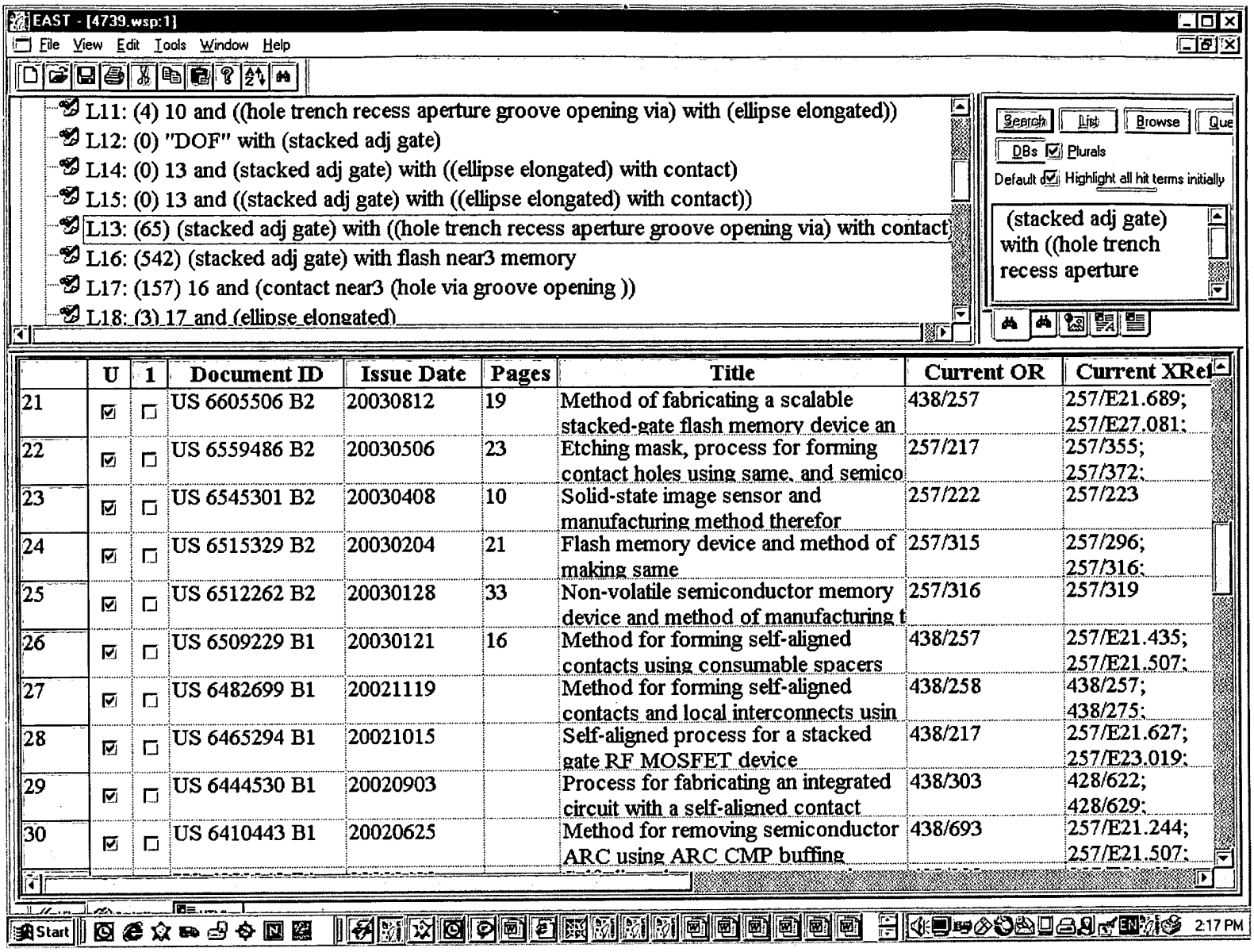
File View Edit Tools Window Help

L11: (4) 10 and ((hole trench recess aperture groove opening via) with (ellipse elongated))
L12: (0) "DOF" with (stacked adj gate)
L14: (0) 13 and (stacked adj gate) with ((ellipse elongated) with contact)
L15: (0) 13 and ((stacked adj gate) with ((ellipse elongated) with contact))
L13: (65) (stacked adj gate) with ((hole trench recess aperture groove opening via) with contact
L16: (542) (stacked adj gate) with flash near3 memory
L17: (157) 16 and (contact near3 (hole via groove opening))
L18: (3) 17 and (ellipse elongated)

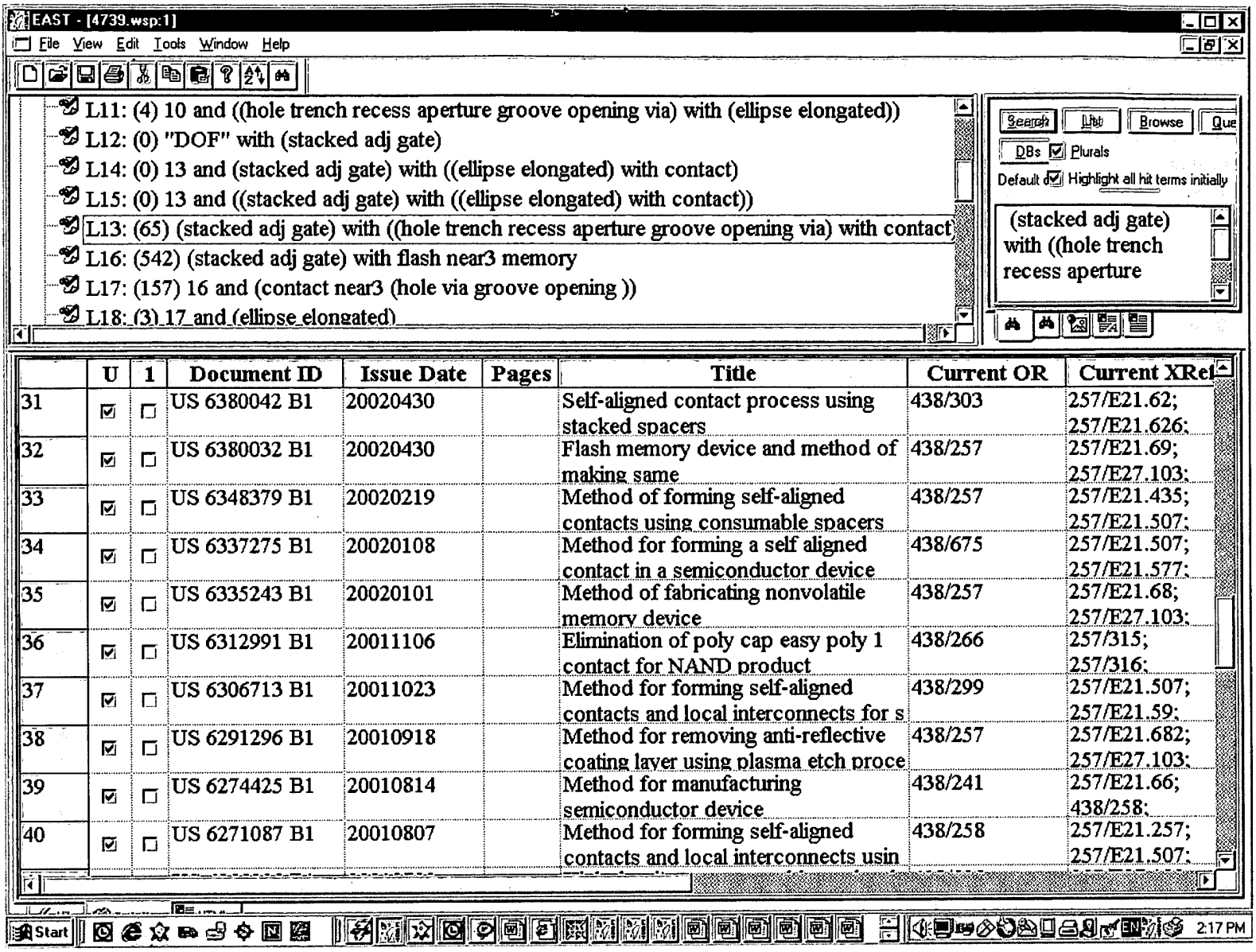
Search | List | Browse | Que
DBs ☑ Plurals
Default ☑ Highlight all hit terms initially
(stacked adj gate) with ((hole trench recess aperture

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
11	☑	☐	US 20020072167 A1	20020613	21	Flash memory device and method of making same	438/201	257/E21.69; 257/E27.103;
12	☑	☐	US 20020034856 A1	20020321	12	Method for forming junction electrode of semiconductor device	438/381	257/E21.166; 257/E21.171;
13	☑	☐	US 20020017692 A1	20020214	24	Non-volatile semiconductor memory device having memory cell array suita	257/390	257/758; 257/E21.682;
14	☑	☐	US 20010045585 A1	20011129	35	NON-VOLATILE SEMICONDUCTOR MEMORY DE	257/296	
15	☑	☐	US 20010031524 A1	20011018	16	Nonvolatile memory device and manufacturing method therefor	438/201	257/E21.683; 257/E27.081;
16	☑	☐	US 20010015428 A1	20010823	11	Solid-state image sensor and manufacturing method therefor	257/1	
17	☑	☐	US 20010002731 A1	20010607	24	Etching mask, process for forming contact holes using same, and semico	257/750	257/759; 257/760;
18	☑	☐	US 6713388 B2	20040330	12	Method of fabricating a non-volatile memory device to eliminate charge lo	438/673	438/639
19	☑	☐	US 6667220 B2	20031223	12	Method for forming junction electrode of semiconductor device	438/400	257/E21.166; 257/E21.171;
20	☑	☐	US 6667211 B2	20031223	33	Non-volatile semiconductor memory device and method of manufacturing t	438/259	438/258; 438/589;

Start 2:17 PM



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
21	☑	☐	US 6605506 B2	20030812	19	Method of fabricating a scalable stacked-gate flash memory device an	438/257	257/E21.689; 257/E27.081;
22	☑	☐	US 6559486 B2	20030506	23	Etching mask, process for forming contact holes using same, and semico	257/217	257/355; 257/372;
23	☑	☐	US 6545301 B2	20030408	10	Solid-state image sensor and manufacturing method therefor	257/222	257/223
24	☑	☐	US 6515329 B2	20030204	21	Flash memory device and method of making same	257/315	257/296; 257/316;
25	☑	☐	US 6512262 B2	20030128	33	Non-volatile semiconductor memory device and method of manufacturing t	257/316	257/319
26	☑	☐	US 6509229 B1	20030121	16	Method for forming self-aligned contacts using consumable spacers	438/257	257/E21.435; 257/E21.507;
27	☑	☐	US 6482699 B1	20021119		Method for forming self-aligned contacts and local interconnects usin	438/258	438/257; 438/275;
28	☑	☐	US 6465294 B1	20021015		Self-aligned process for a stacked gate RF MOSFET device	438/217	257/E21.627; 257/E23.019;
29	☑	☐	US 6444530 B1	20020903		Process for fabricating an integrated circuit with a self-aligned contact	438/303	428/622; 428/629;
30	☑	☐	US 6410443 B1	20020625		Method for removing semiconductor ARC using ARC CMP buffing	438/693	257/E21.244; 257/E21.507;



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
31	☑	☐	US 6380042 B1	20020430		Self-aligned contact process using stacked spacers	438/303	257/E21.62; 257/E21.626;
32	☑	☐	US 6380032 B1	20020430		Flash memory device and method of making same	438/257	257/E21.69; 257/E27.103;
33	☑	☐	US 6348379 B1	20020219		Method of forming self-aligned contacts using consumable spacers	438/257	257/E21.435; 257/E21.507;
34	☑	☐	US 6337275 B1	20020108		Method for forming a self aligned contact in a semiconductor device	438/675	257/E21.507; 257/E21.577;
35	☑	☐	US 6335243 B1	20020101		Method of fabricating nonvolatile memory device	438/257	257/E21.68; 257/E27.103;
36	☑	☐	US 6312991 B1	20011106		Elimination of poly cap easy poly 1 contact for NAND product	438/266	257/315; 257/316;
37	☑	☐	US 6306713 B1	20011023		Method for forming self-aligned contacts and local interconnects for s	438/299	257/E21.507; 257/E21.59;
38	☑	☐	US 6291296 B1	20010918		Method for removing anti-reflective coating layer using plasma etch proce	438/257	257/E21.682; 257/E27.103;
39	☑	☐	US 6274425 B1	20010814		Method for manufacturing semiconductor device	438/241	257/E21.66; 438/258;
40	☑	☐	US 6271087 B1	20010807		Method for forming self-aligned contacts and local interconnects usin	438/258	257/E21.257; 257/E21.507;

EAST - [4739.wsp:1]

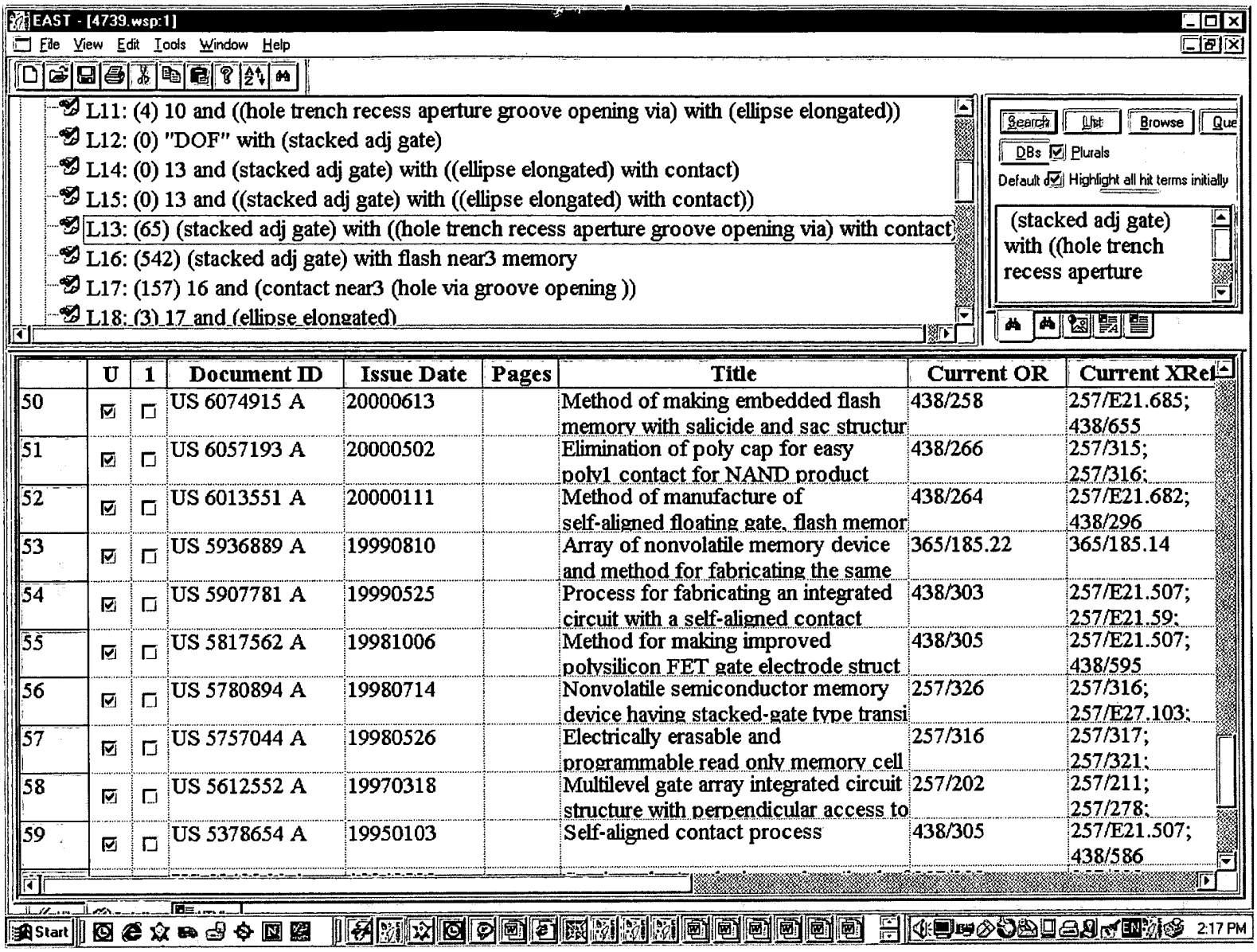
File View Edit Tools Window Help

L11: (4) 10 and ((hole trench recess aperture groove opening via) with (ellipse elongated))
L12: (0) "DOF" with (stacked adj gate)
L14: (0) 13 and (stacked adj gate) with ((ellipse elongated) with contact)
L15: (0) 13 and ((stacked adj gate) with ((ellipse elongated) with contact))
L13: (65) (stacked adj gate) with ((hole trench recess aperture groove opening via) with contact
L16: (542) (stacked adj gate) with flash near3 memory
L17: (157) 16 and (contact near3 (hole via groove opening))
L18: (3) 17 and (ellipse elongated)

Search | List | Browse | Que
DBs ☑ Plurals
Default ☑ Highlight all hit terms initially
(stacked adj gate) with ((hole trench recess aperture

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
41	☑	☐	US 6255205 B1	20010703		High density programmable read-only memory employing double-wall space	438/595	257/E27.103; 438/266
42	☑	☐	US 6240021 B1	20010529		Nonvolatile semiconductor memory device improved in readout operation	365/185.27	365/185.18
43	☑	☐	US 6221777 B1	20010424		Reverse lithographic process for semiconductor vias	438/692	257/E21.577; 257/E21.682;
44	☑	☐	US 6204161 B1	20010320		Self aligned contact pad in a semiconductor device and method fo	438/612	257/E21.507; 257/E21.576;
45	☑	☐	US 6190968 B1	20010220		Method for forming EPROM and flash memory cells with source-side i	438/259	257/E21.682; 257/E29.306
46	☑	☐	US 6180454 B1	20010130		Method for forming flash memory devices	438/257	438/266; 438/593
47	☑	☐	US 6172395 B1	20010109		Method of manufacture of self-aligned floating gate, flash memor	257/315	257/346; 257/401;
48	☑	☐	US 6136649 A	20001024		Method for removing anti-reflective coating layer using plasma etch proce	438/257	257/E21.422; 257/E21.682;
49	☑	☐	US 6133096 A	20001017		Process for simultaneously fabricating a stack gate flash memory	438/264	257/E21.684; 257/E27.081;
50	☑	☐	US 6074915 A	20000613		Method of making embedded flash memory with salicide and sac structur	438/258	257/E21.685; 438/655

Start 2:17 PM



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
50	☑	☐	US 6074915 A	20000613		Method of making embedded flash memory with salicide and sac structur	438/258	257/E21.685; 438/655
51	☑	☐	US 6057193 A	20000502		Elimination of poly cap for easy poly1 contact for NAND product	438/266	257/315; 257/316;
52	☑	☐	US 6013551 A	20000111		Method of manufacture of self-aligned floating gate, flash memor	438/264	257/E21.682; 438/296
53	☑	☐	US 5936889 A	19990810		Array of nonvolatile memory device and method for fabricating the same	365/185.22	365/185.14
54	☑	☐	US 5907781 A	19990525		Process for fabricating an integrated circuit with a self-aligned contact	438/303	257/E21.507; 257/E21.59;
55	☑	☐	US 5817562 A	19981006		Method for making improved polysilicon FET gate electrode struct	438/305	257/E21.507; 438/595
56	☑	☐	US 5780894 A	19980714		Nonvolatile semiconductor memory device having stacked-gate type transi	257/326	257/316; 257/E27.103;
57	☑	☐	US 5757044 A	19980526		Electrically erasable and programmable read only memory cell	257/316	257/317; 257/321;
58	☑	☐	US 5612552 A	19970318		Multilevel gate array integrated circuit structure with perpendicular access to	257/202	257/211; 257/278;
59	☑	☐	US 5378654 A	19950103		Self-aligned contact process	438/305	257/E21.507; 438/586